

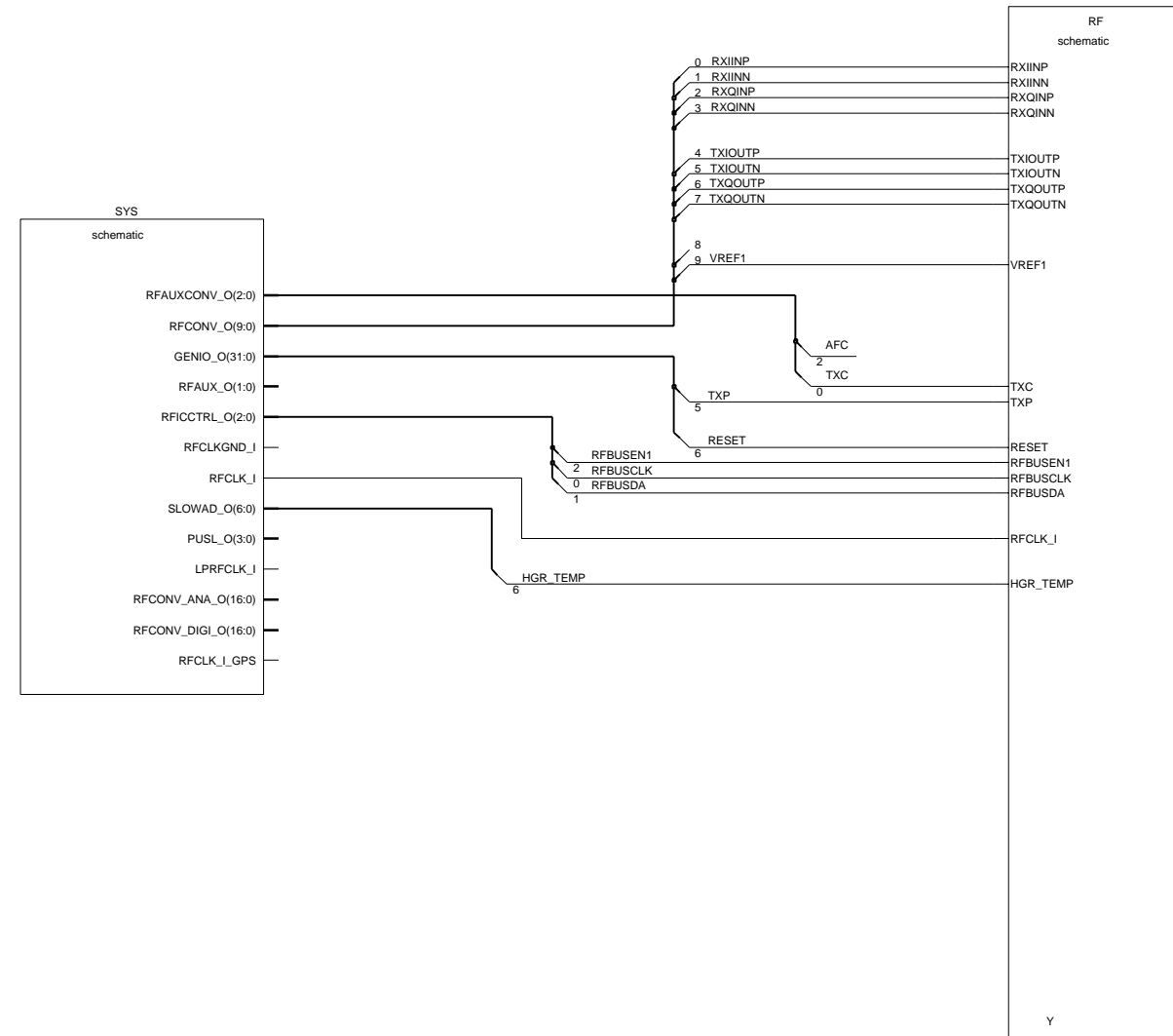
8 - SCHEMATICS

Table of Contents

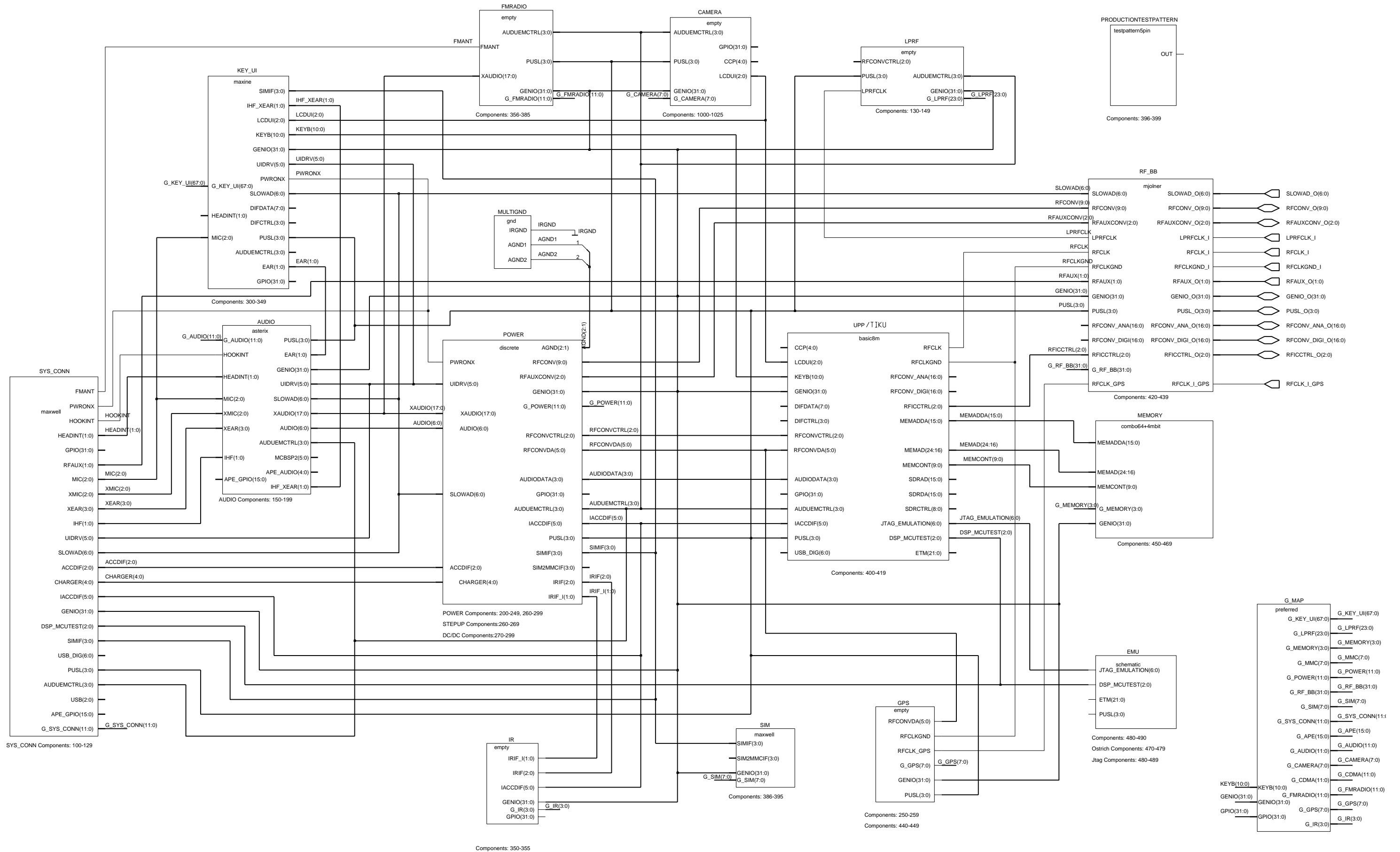
	Page No
Schematics (Table of Contents) .....	1
Top sheet .....	2
DCT4 Common Baseband Schematic (Top Level) .....	3
RH-19/RH-50 System Connector.....	4
RH-19/RH-50 User Interface.....	5
RH-19/RH-50 Audio.....	6
MultiGND symbol bypass .....	7
5 pin Production Test Pattern .....	7
Discrete Power Management .....	8
Light filtering .....	9
DC/DC Converter .....	10
PWR resistor 0805 thermal1 .....	10
SIM reader for RH-19/RH-50.....	10
RH-19/RH-50 Filters / No IR Interface present in this product.....	11
Module ID .....	11
UPP 8M Implementation .....	12
Discrete decoupling capacitors for UPP .....	13
Testpoints based Ostrich Interface .....	13
GSM RF - Baseband Interface .....	14
Combo Memory 64 + 4 Mbit .....	15
Discrete capacitors for memory without VFlash1 .....	16
Empty wing sheet .....	16
Test and Emulator Interface .....	17
Testpoints for JTAG Emulator .....	18
RF Top sheet .....	19
Power Amplifier .....	20
Mjoelner .....	21
Component layout diagram, top.....	22
Component layout diagram, bottom.....	23

Title: Top Sheet

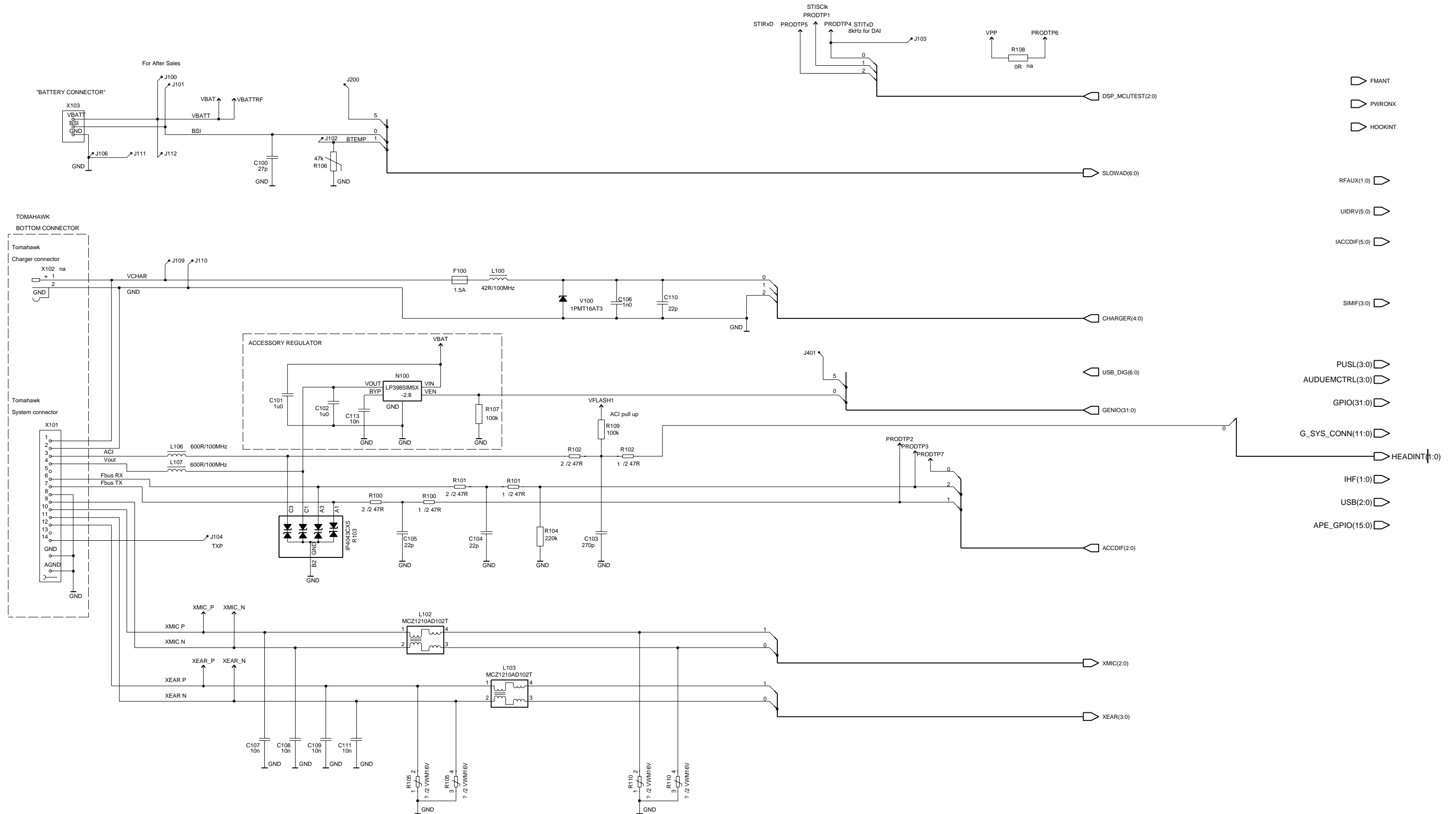
CBB_OVERVIEW		MODEL	CBB_VERSION
SYS_CONN		MAXWELL	SYS_6.1
KEY_UI		MAXINE	SYS_6.1
AUDIO		MAXWELL	SYS_6.1
FMRADIO		EMPTY	SYS_6.1
MULTIGND		GND	SYS_6.1
POWER	PWRFILTER	DISCRETE	SYS_6.1
	DC_DC	LIGHT	SYS_6.1
	REG_CAP	EMPTY	SYS_6.1
	PWR_RES	MAXWELL	SYS_6.1
		THERM1	SYS_6.1
IR		EMPTY	SYS_6.1
CAMERA		EMPTY	SYS_6.1
LPRF		EMPTY	SYS_6.1
UPP	UPPFILTER	BASIC8M	SYS_6.1
		DISCRETE	SYS_6.1
SIM		MAXWELL	SYS_6.1
GPS		EMPTY	SYS_6.1
PRODUCTIONS PATTERN	MODULE_ID	TESTPATTERN SPIN	SYS_6.1
		MODULE_ID	SYS_6.1
RF_BB		MJOLNER	SYS_6.1
MEMORY	MEMFILTER MEMWING MEMEXTENSION	COMBO64+4MBIT	SYS_6.1
		NOVFLASH1CAP	SYS_6.1
		EMPTY	SYS_6.1
		EMPTY	SYS_6.1
EMU	JTAG OSTRICH ETM	SCHEMATIC	SYS_6.1
		TESTPOINT	SYS_6.1
		TESTPOINT	SYS_6.1
		EMPTY	SYS_6.1



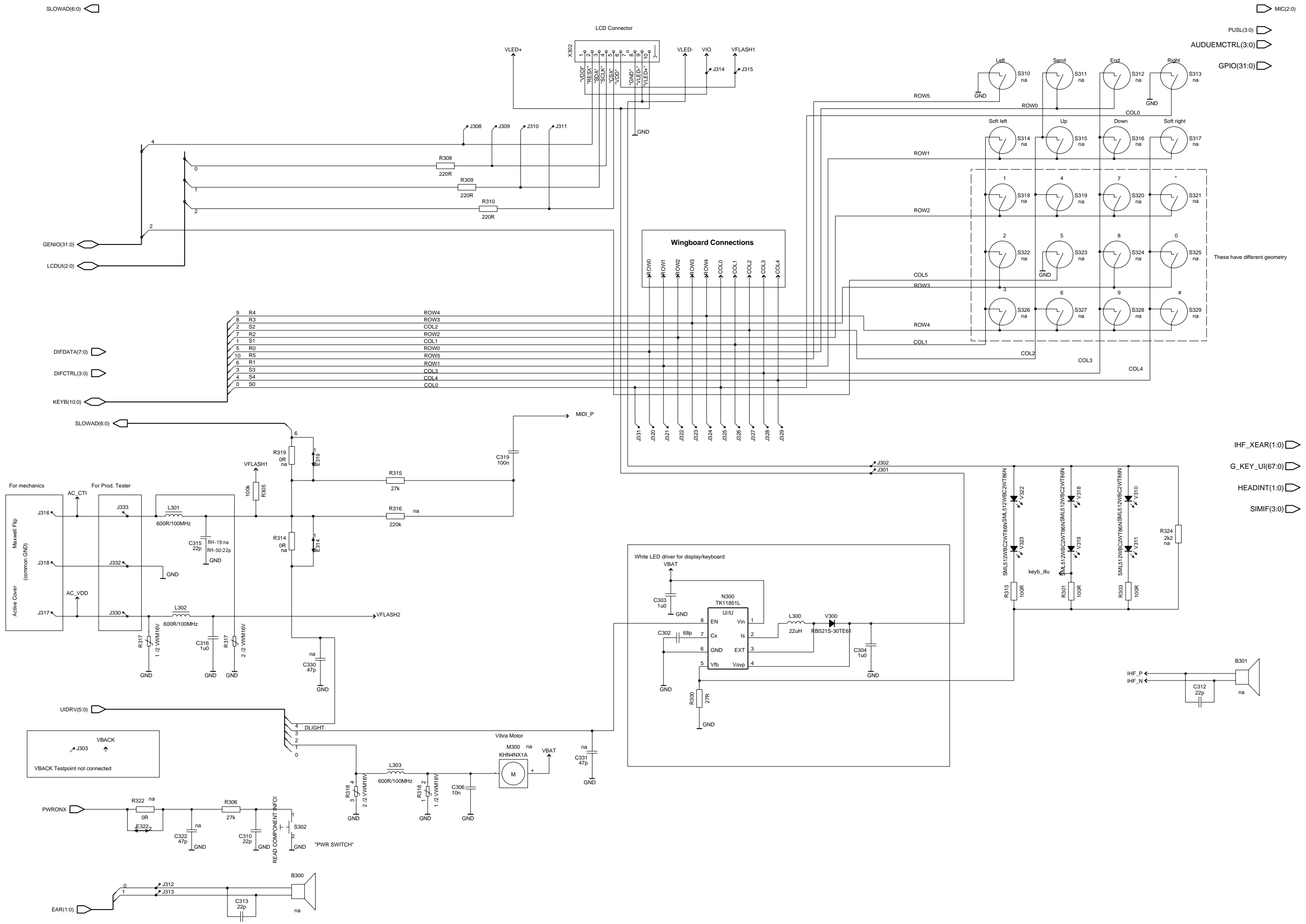
Title: DCT4 Common Baseband Schematic (Top Level)



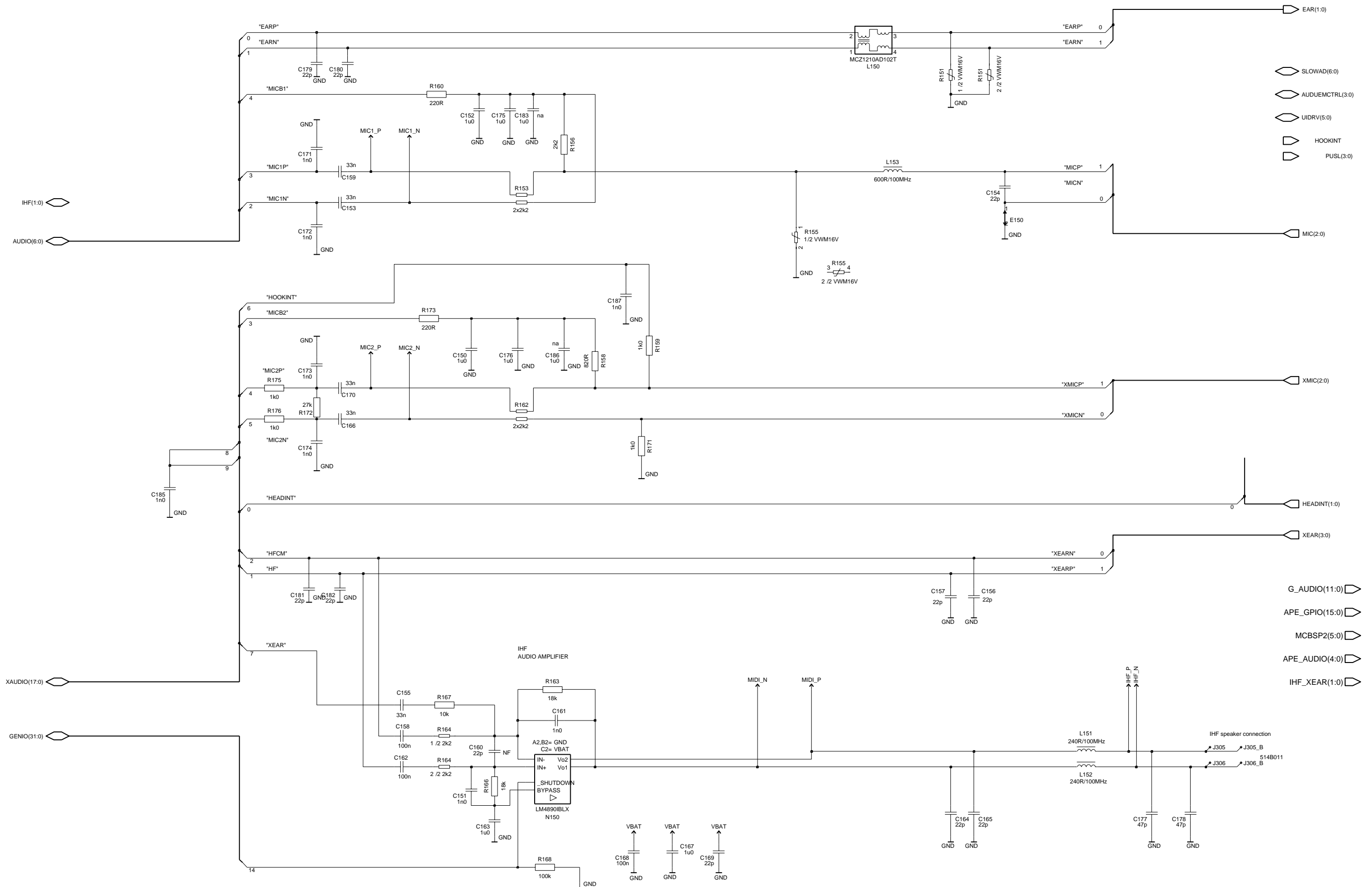
Title: RH-19/RH-50 System Connector



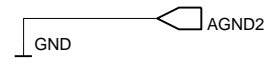
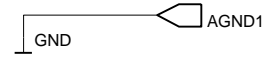
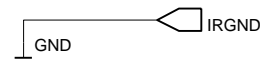
Title: RH-19/RH-50 User Interface



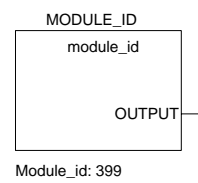
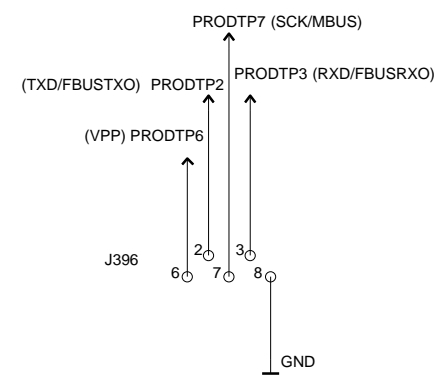
Title: RH-19/RH-50 Audio



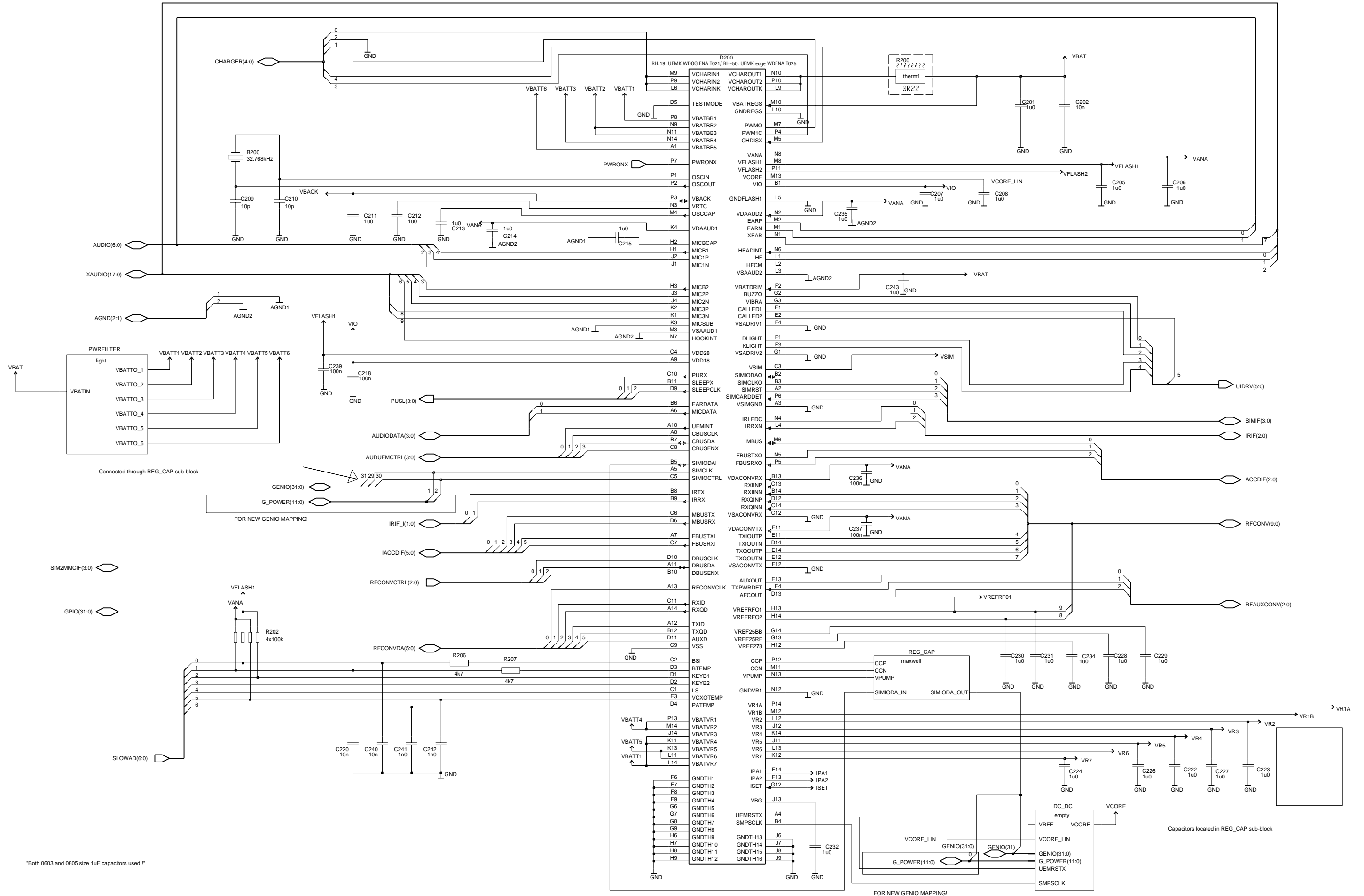
Title: MultiGND Symbol Bypass



Title: 5 pin Production Test Pattern

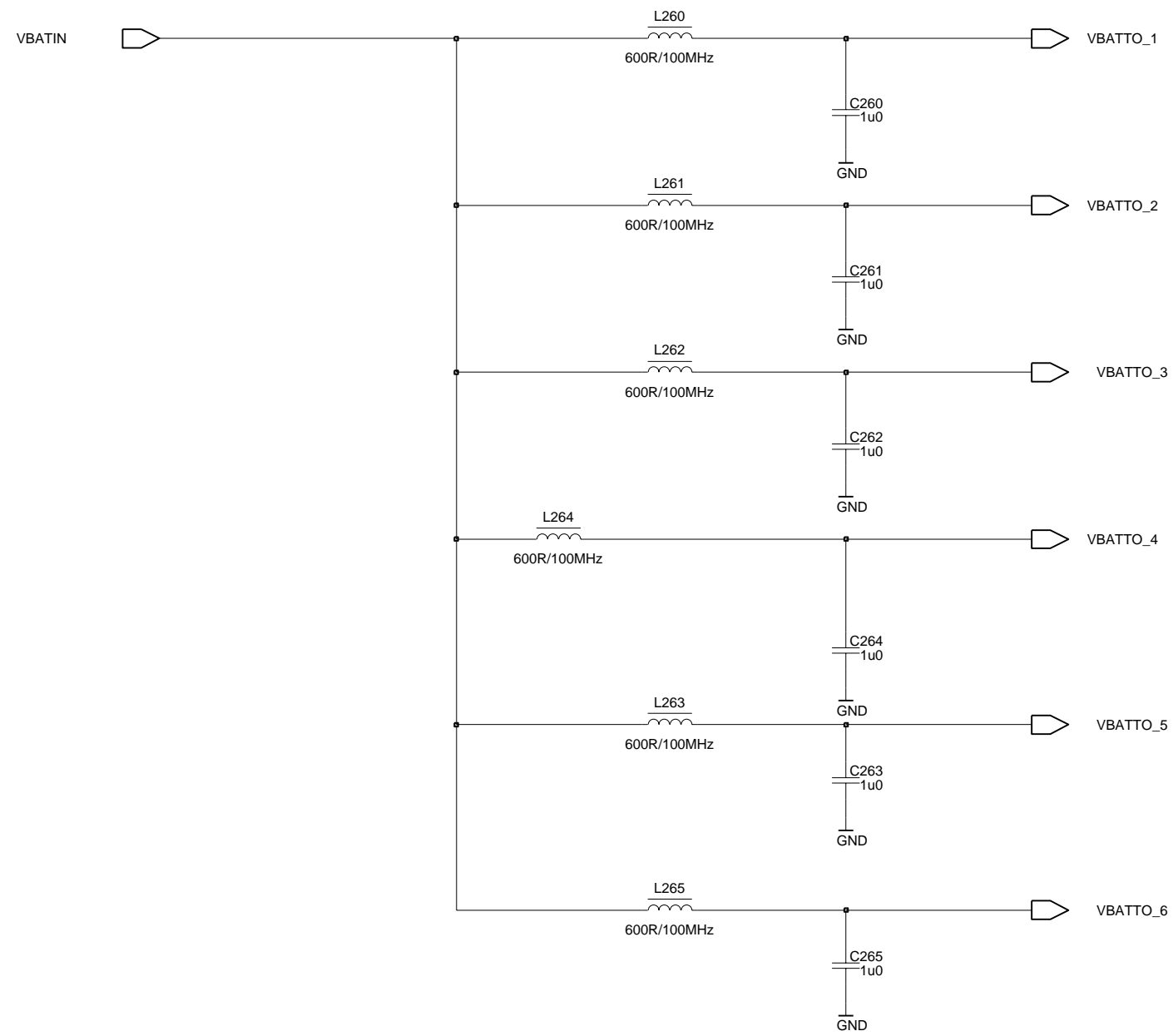


Title: Discrete Power Management

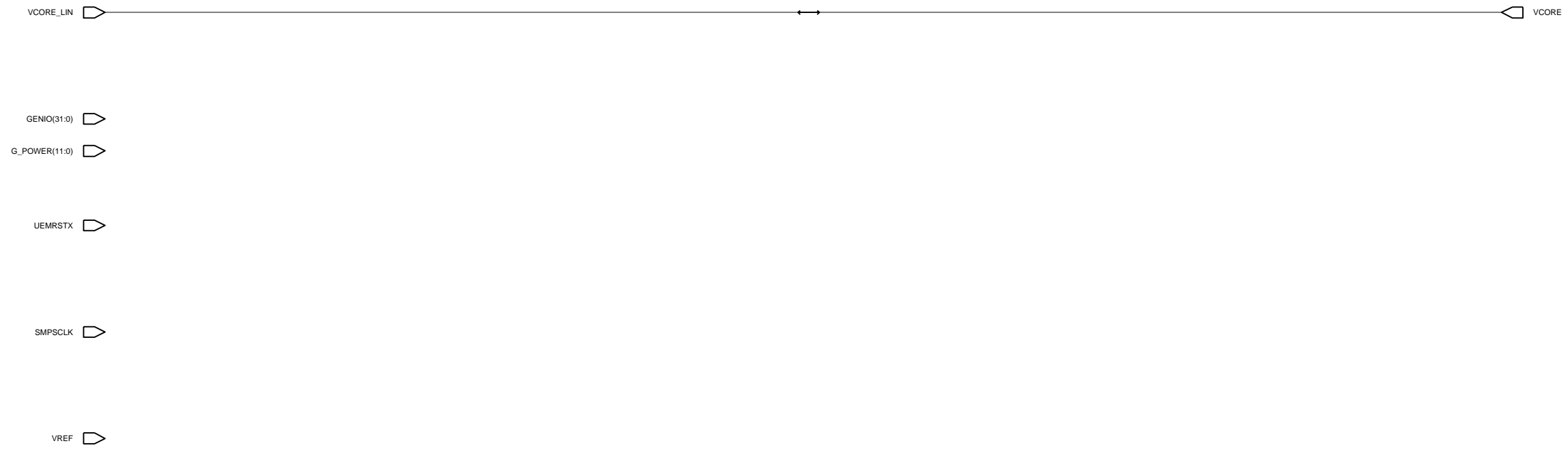




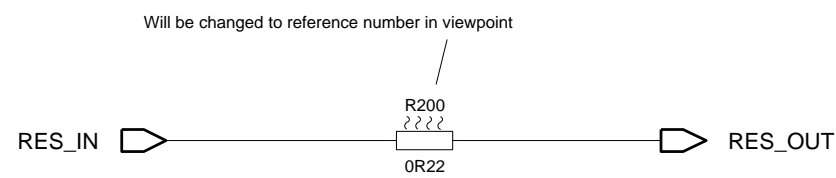
Title: Light Filtering



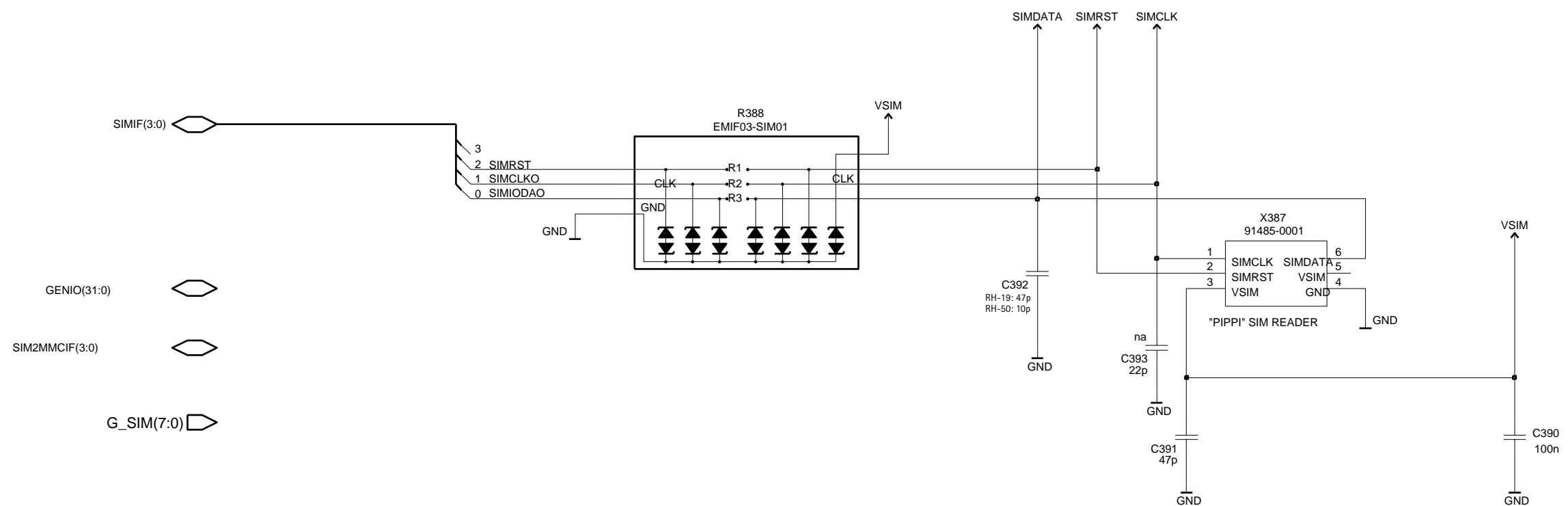
Title: DC/DC Convertor



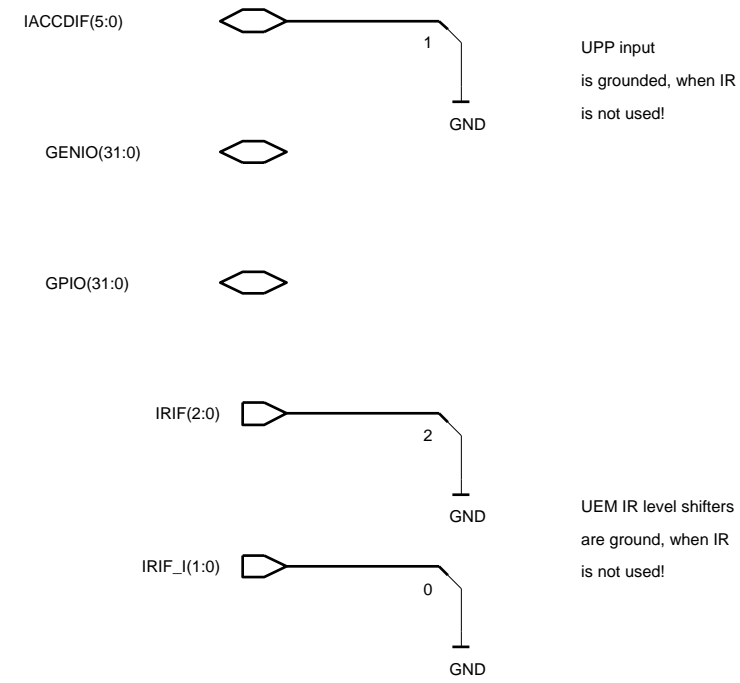
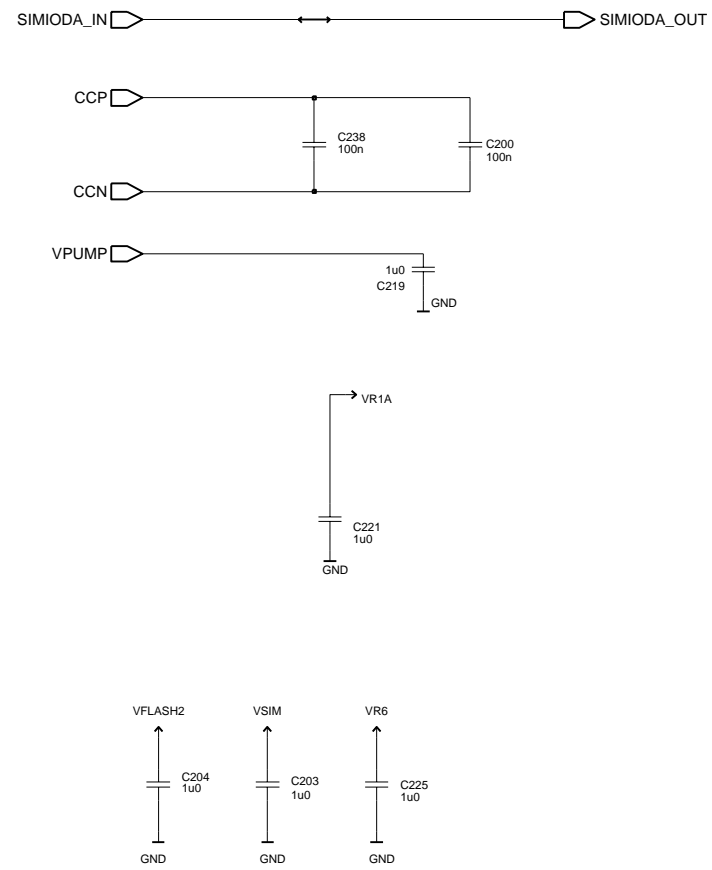
Title: PWR Resistor 0805 thermal1



Title: SIM Reader for RH-19/RH-50

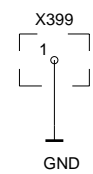


**Title: RH-19/RH-50 Filters / No IR Interface present in this project**

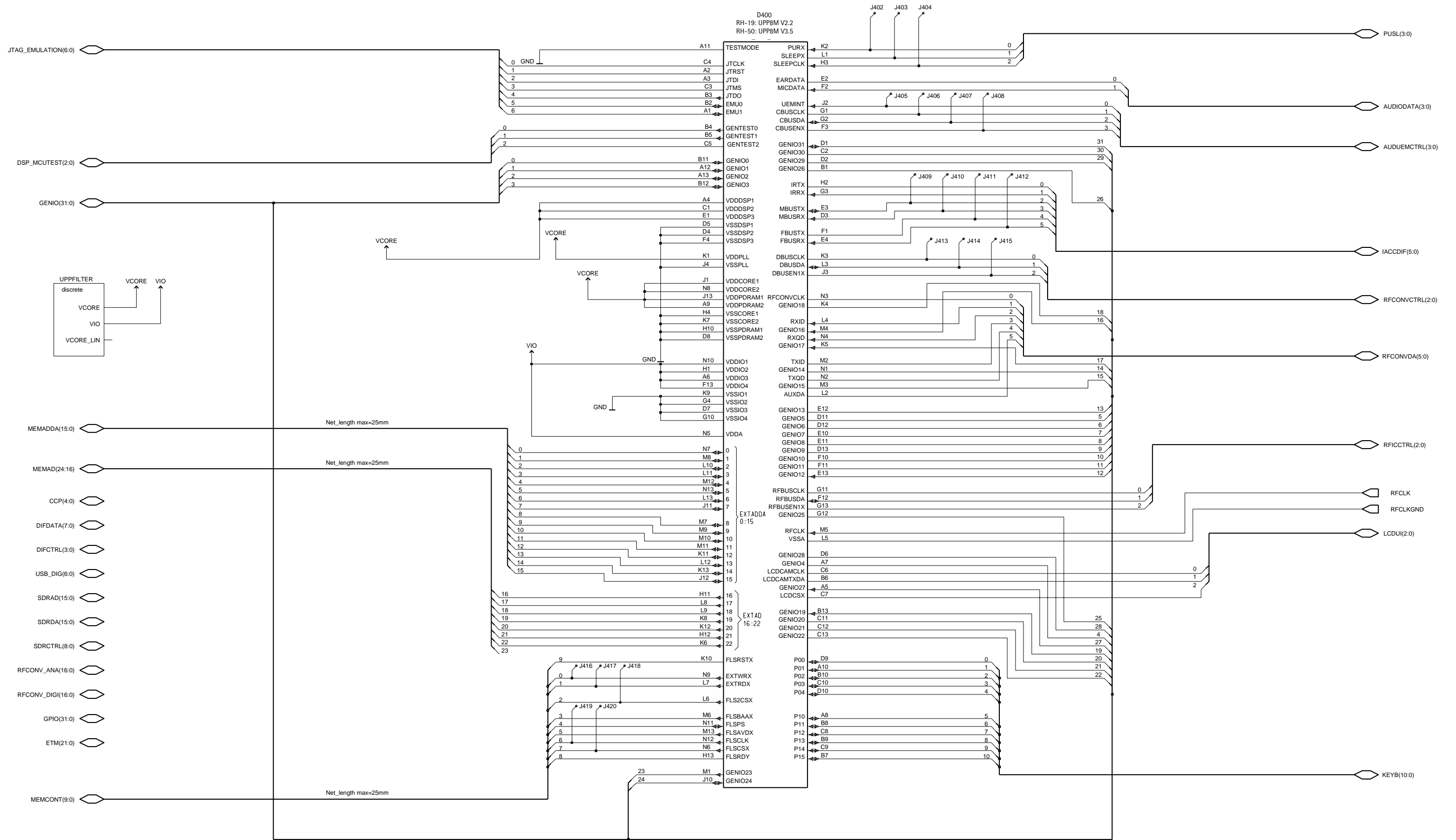


**Title: Module ID**

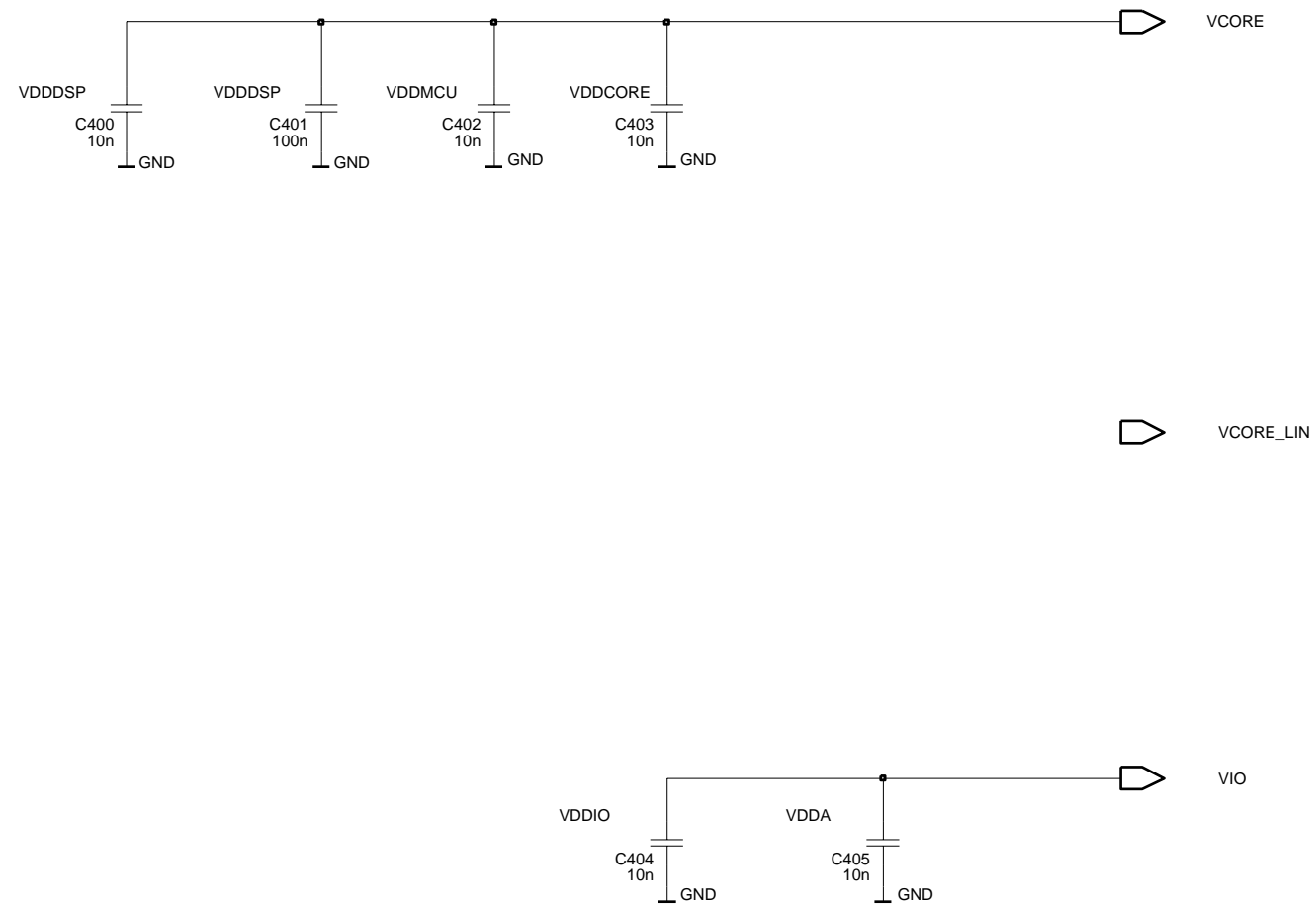
OUTPUT 



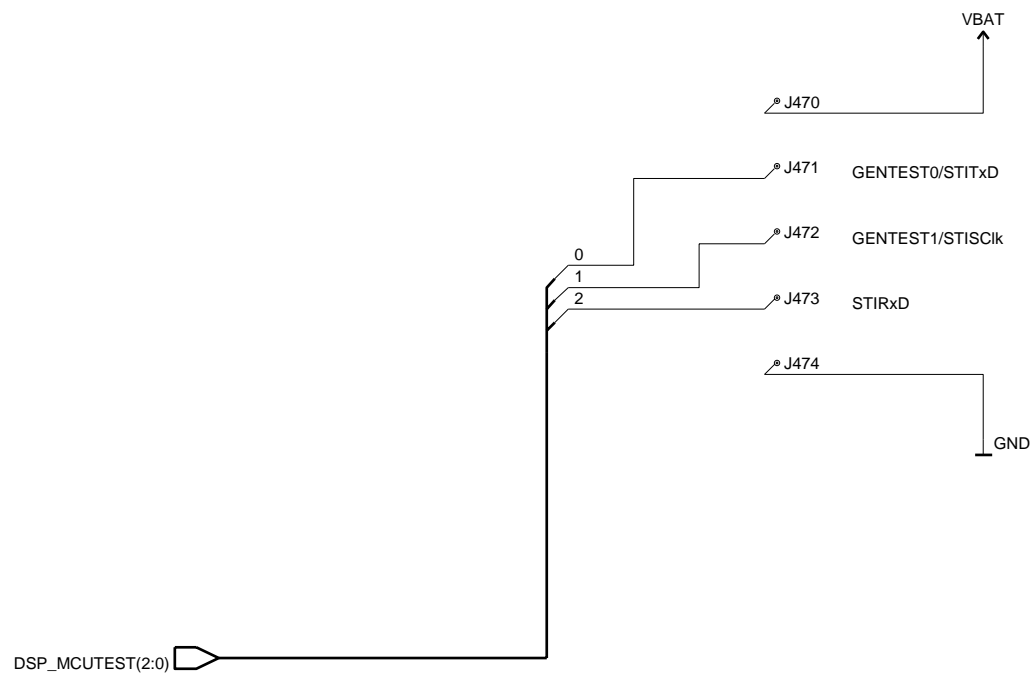
Title: UPP 8M Implementation



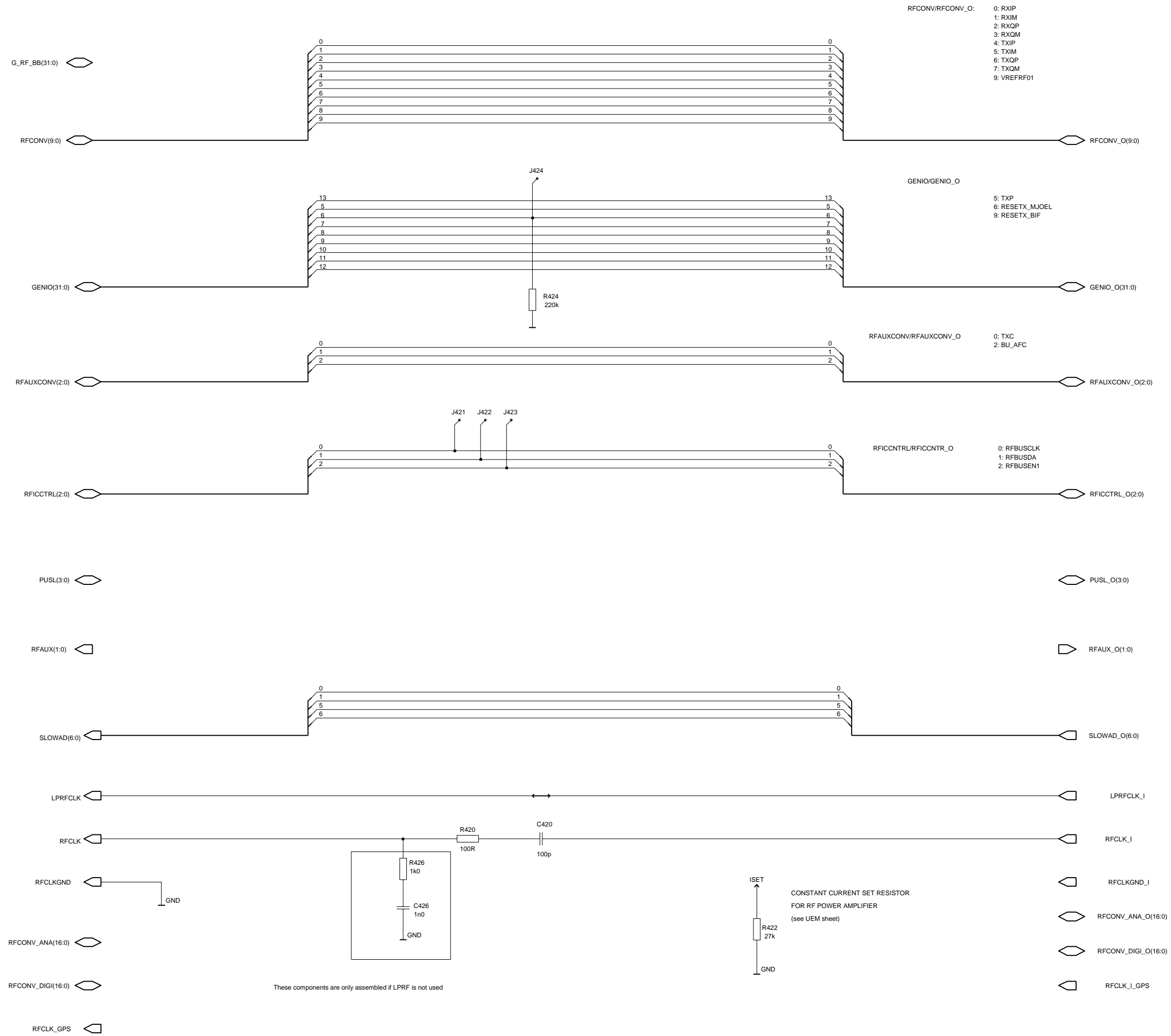
Title: Discrete Decoupling Capacitors for UPP



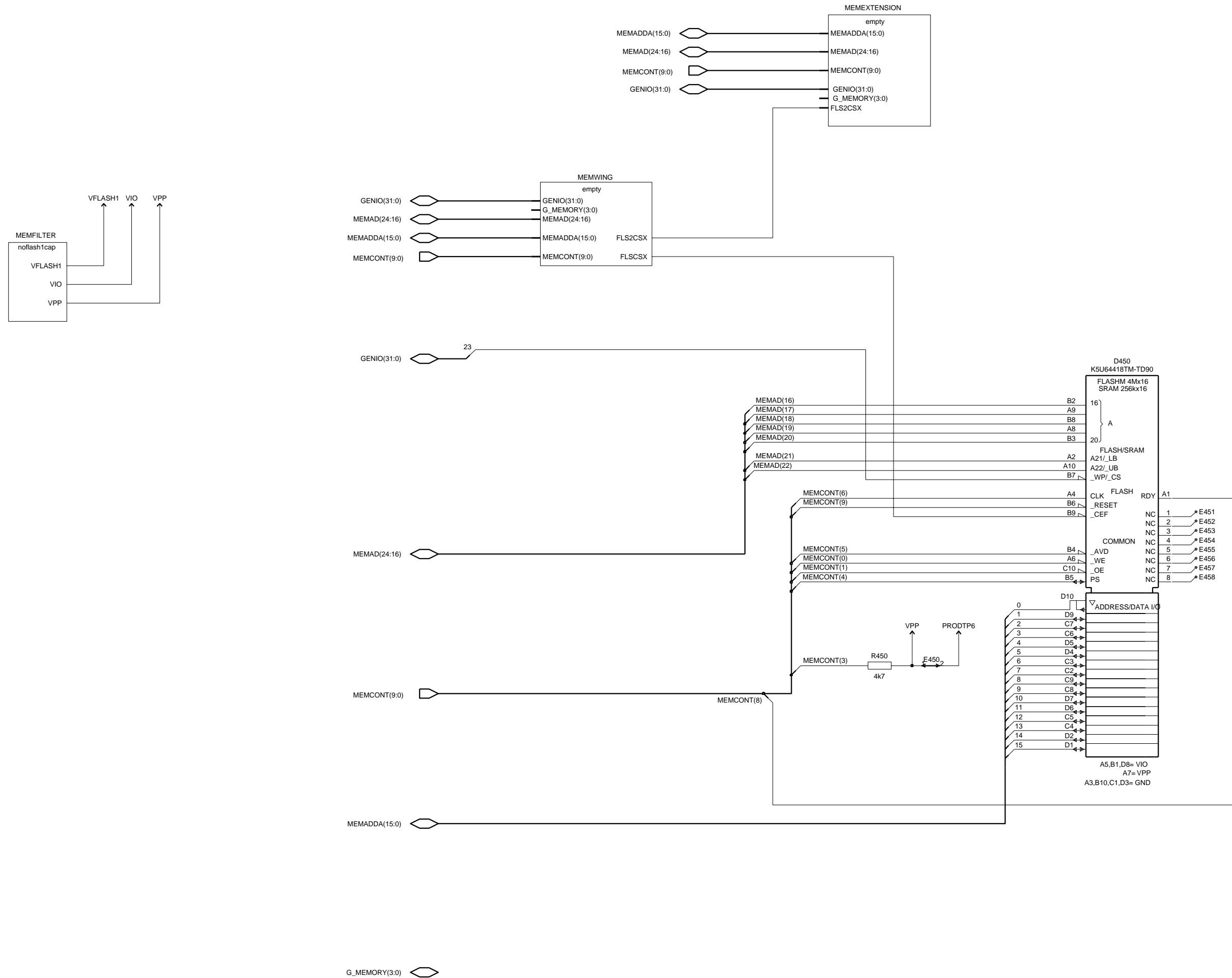
Title: Testpoints based Ostrich Interface



Title: GSM RF - Baseband Interface



Title: Combo Memory 64 + 4 Mbit



Title: Discrete Capacitors for Memory without VFlash1



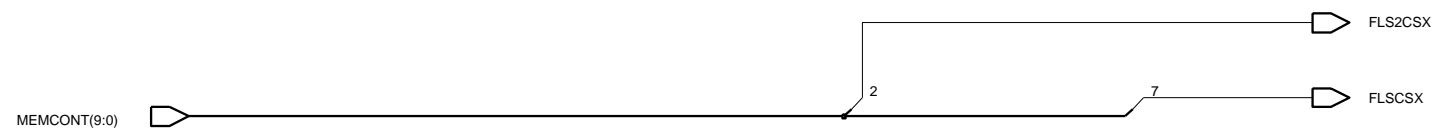
Title: Empty Wing Sheet

MEMADDA(15:0)

MEMAD(24:16)

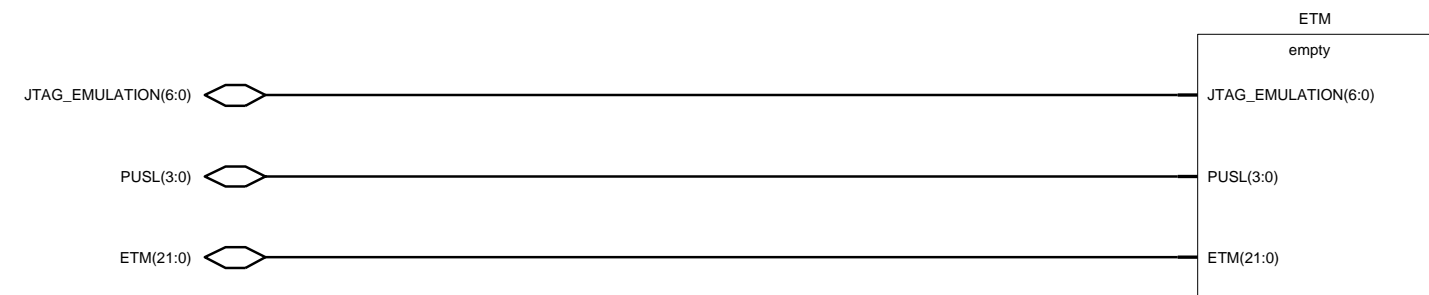
GENIO(31:0)

G\_MEMORY(3:0)

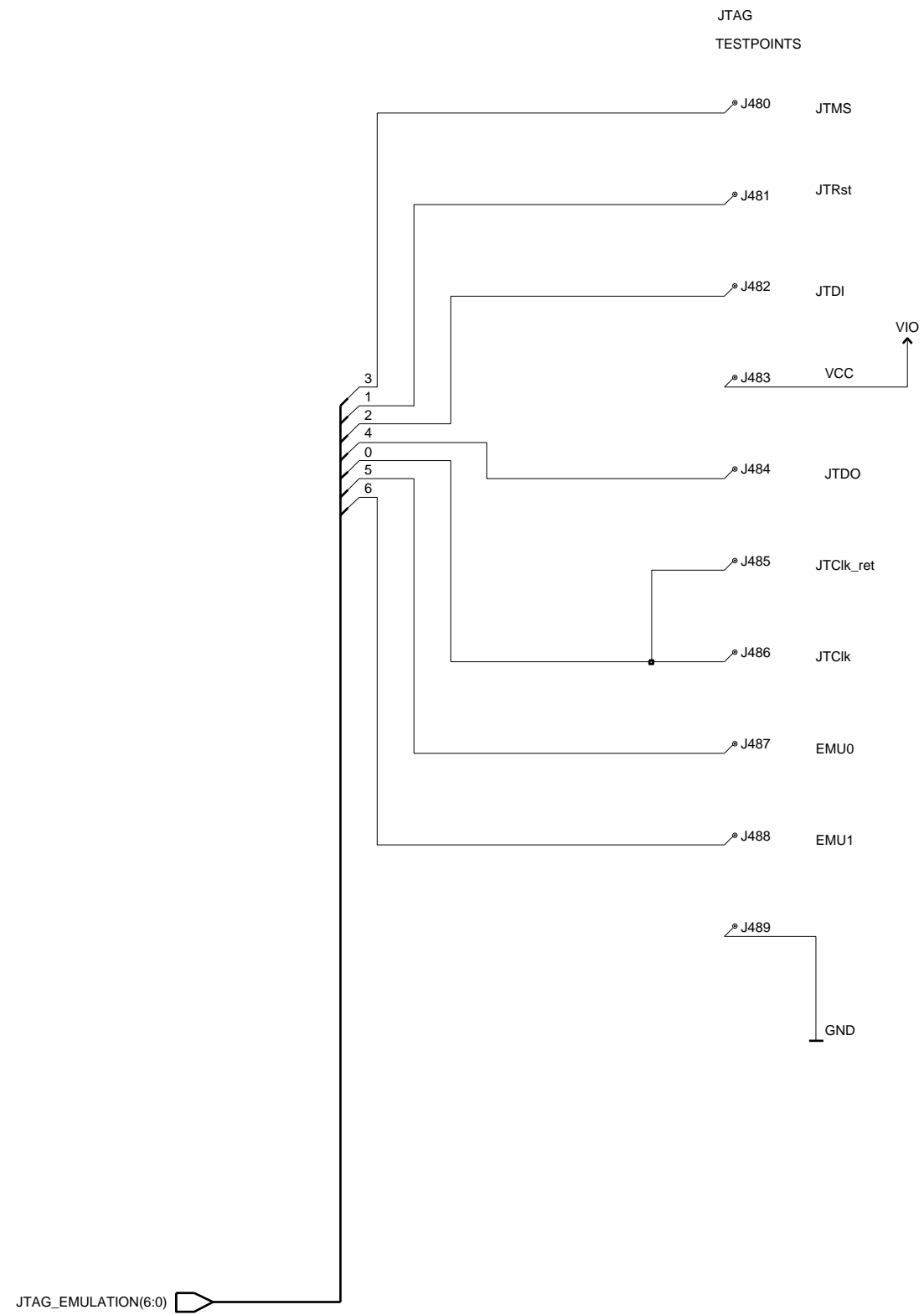




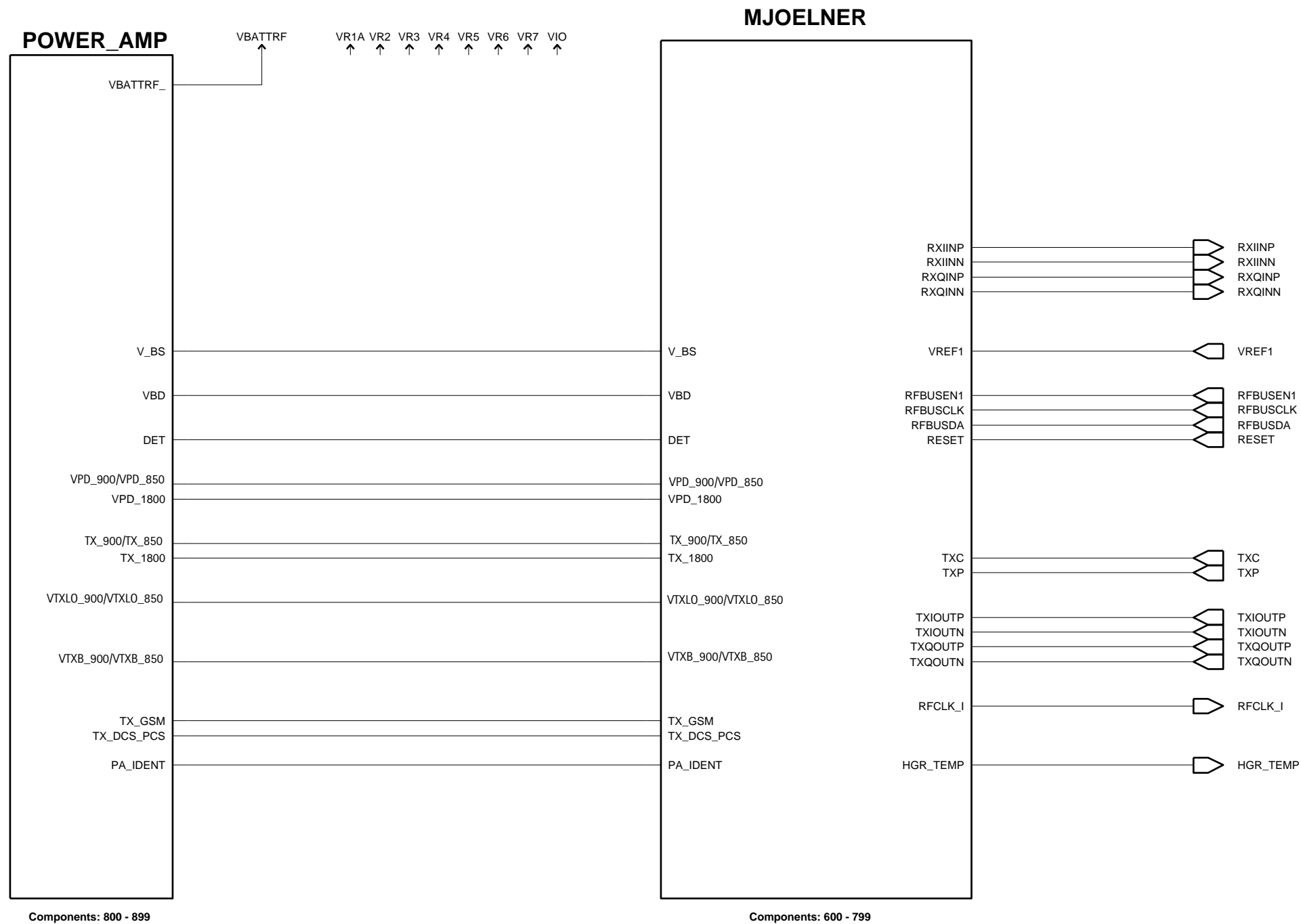
Title: Test and Emulator Interface



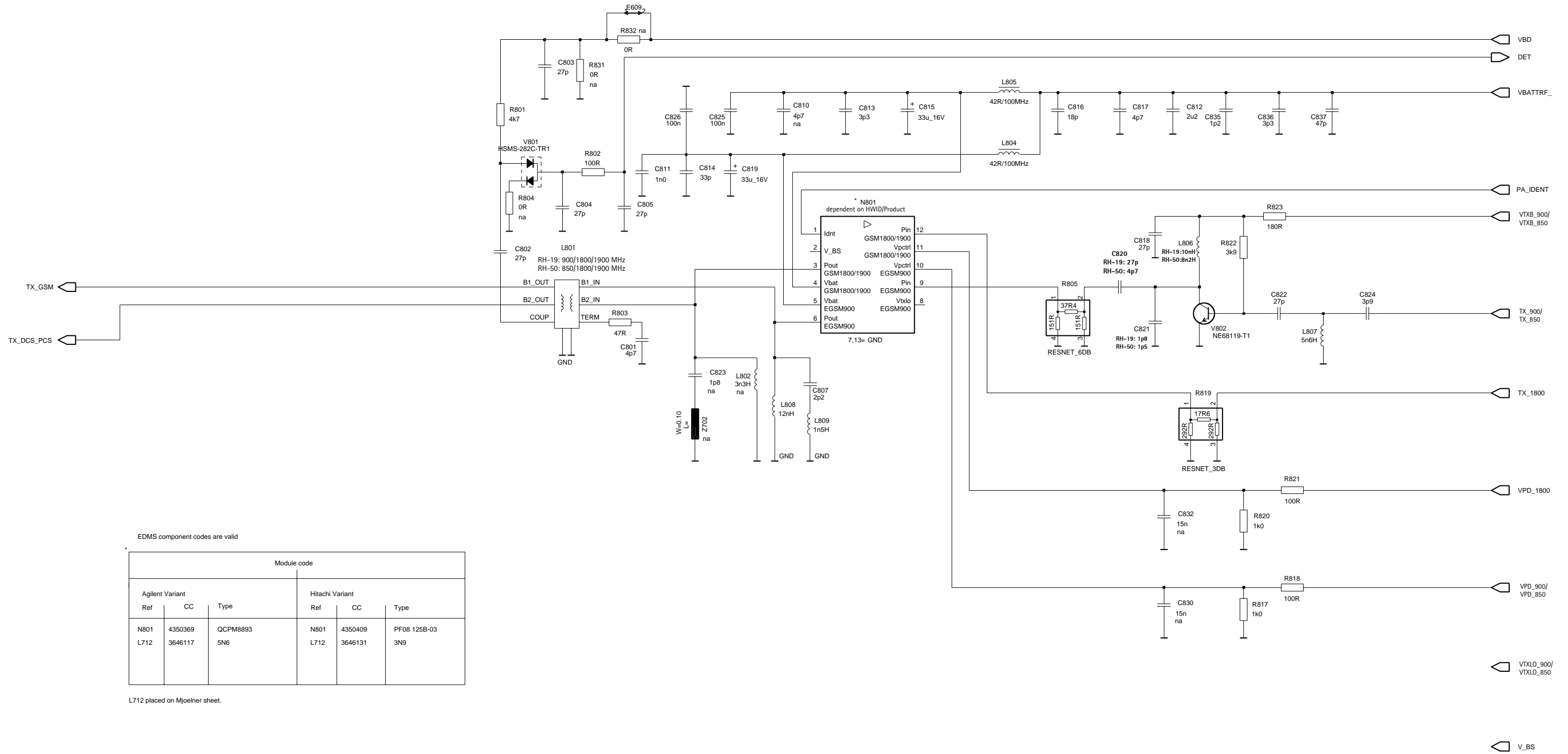
Title: Testpoints for JTAG Emulator



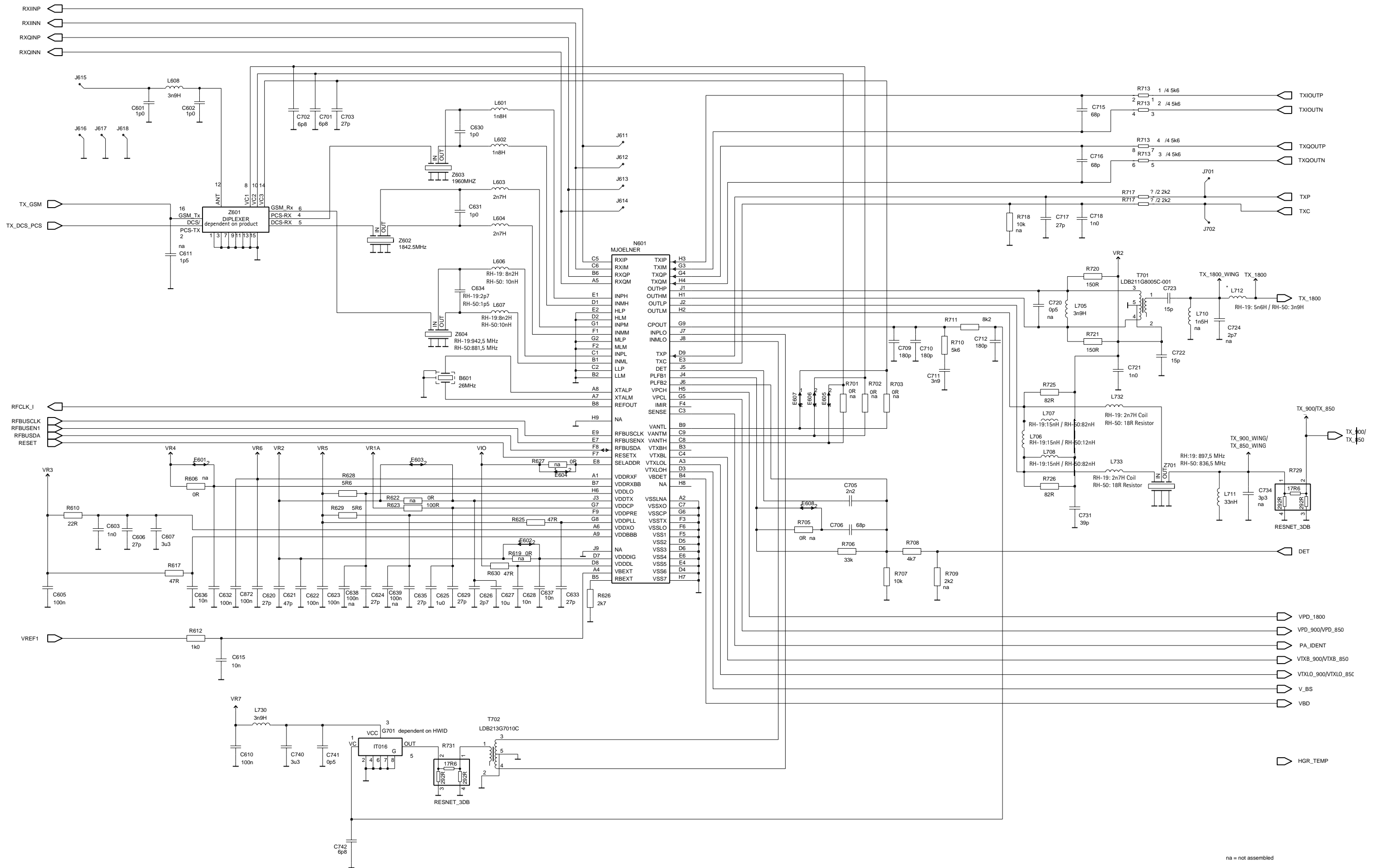
Title: RF Top Sheet



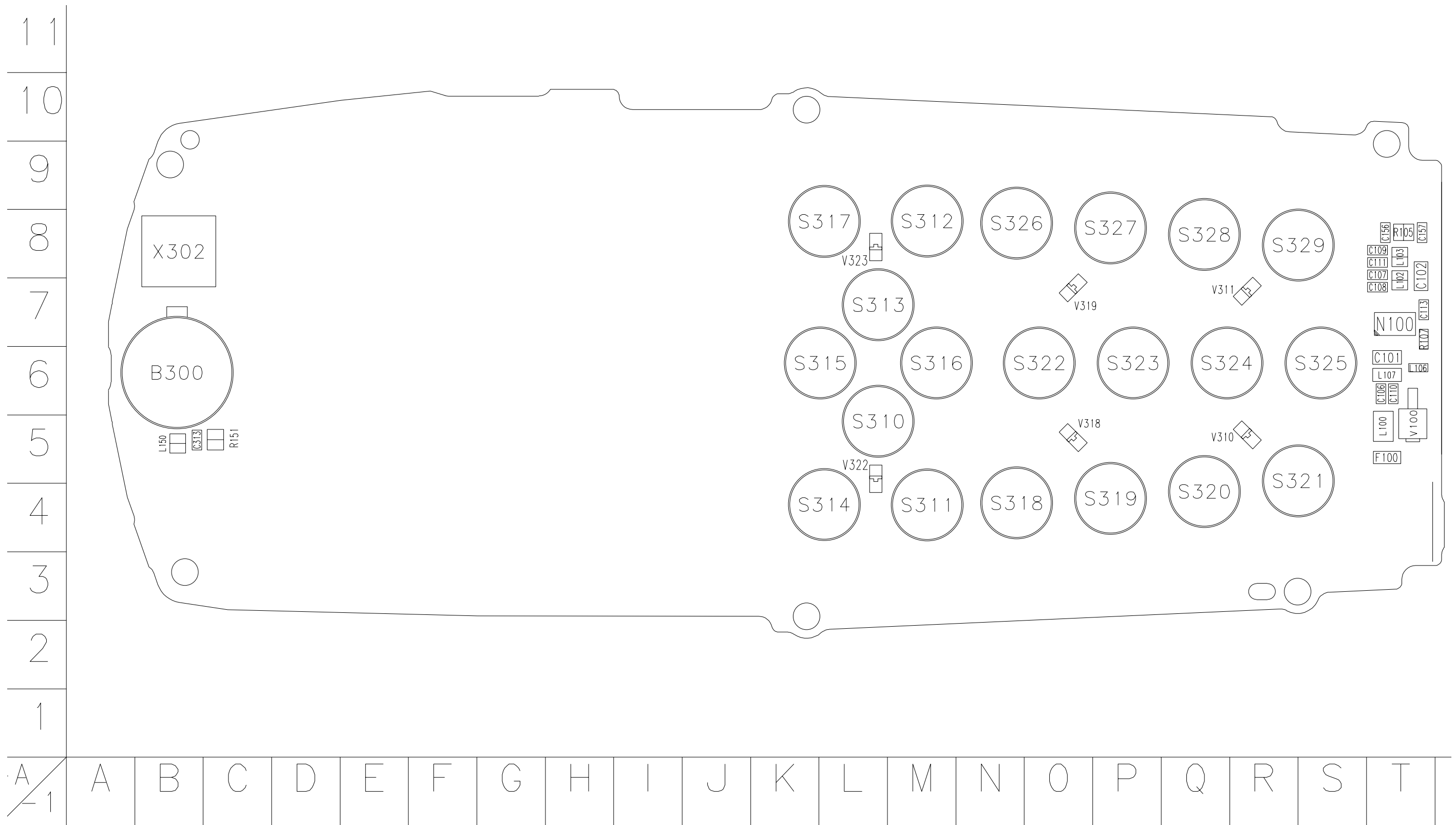
Title: Power Amplifier



Title: Mjoelner



Component layout diagram, top



Component layout diagram, bottom

(Components in red = not assembled)

